Session 130

Using Processor Performance Events to Investigate the Architecture and Tune Applications

Software and Services Group

Phil Kerly

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My Objectives

- Basic understanding how performance counters work
- Strategies/techniques to improve code on Intel-based platforms using performance events
- What it is not…
  - –Tutorial on programming performance event counters

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Top-Down Performance

- System level
  - Process/memory utilization
  - Network
  - Disk and IO
  - Context-switching/paging/system calls
- Application level
  - Parallelism/execution threads
  - Locks
  - APIs
- Microarchitecture level
  - Processor stalls
  - Branch prediction
  - Data and code alignment

Today, Focused on Microarchitecture

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What's a Processor Event

- Counters that detect microarchitectural conditions
  - Occurrences
    - Number of times an event is detected
    - Can occur more than once per cycle
  - Duration
    - Number of cycles an event is detected
  - Conditions (constraints)

Powerful tool to peer inside the architecture

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What Is an "Event Condition"?

Examples

- Only count "Unhalted Clockticks" when in user mode (ring 3)

- Trigger interrupts after 3,000,000 "Unhalted Clockticks" have occurred

- Trigger when no "Instruction Retired" occurs in a given cycle

- Trigger when execution units are idle

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Two Types of Events

- Model-specific events
  - Vast majority of the performance events
  - Tied to the microarchitectural implementation
- Architectural events
  - Behave consistently across microarchitectures
  - Number of events is evolving

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Two Types of Counters

- Fixed counters
  - Instructions retired
  - Unhalted core cycles
  - Unhalted reference cycles
  - Not supported by all Intel processors

- Programmable counters
  - Vast majority of the performance events
  - Tied to the microarchitectural implementation
  - Not all events can be counted on all counters
  - Not all events can be counted at the same time
  - Two or four counters

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Two Basic Modes of Operation

- Counting mode
  - Query processor for the number of event conditions that occurred
  - Don’t correlate with instruction pointer
- Triggering mode
  - Let the processor signal when an event condition occurs
  - Can correlate to instruction pointer for trigger event condition

Enables different sampling methodologies

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Statistical Sampling

- Correlating triggered samples to code
  - Don’t use counter sampling with triggers
- Calibration
  - Not too much, not too little, just right
- Skid
  - Delay between detection and handling interrupt

Results drive analysis—
Bad results can drive wrong conclusions

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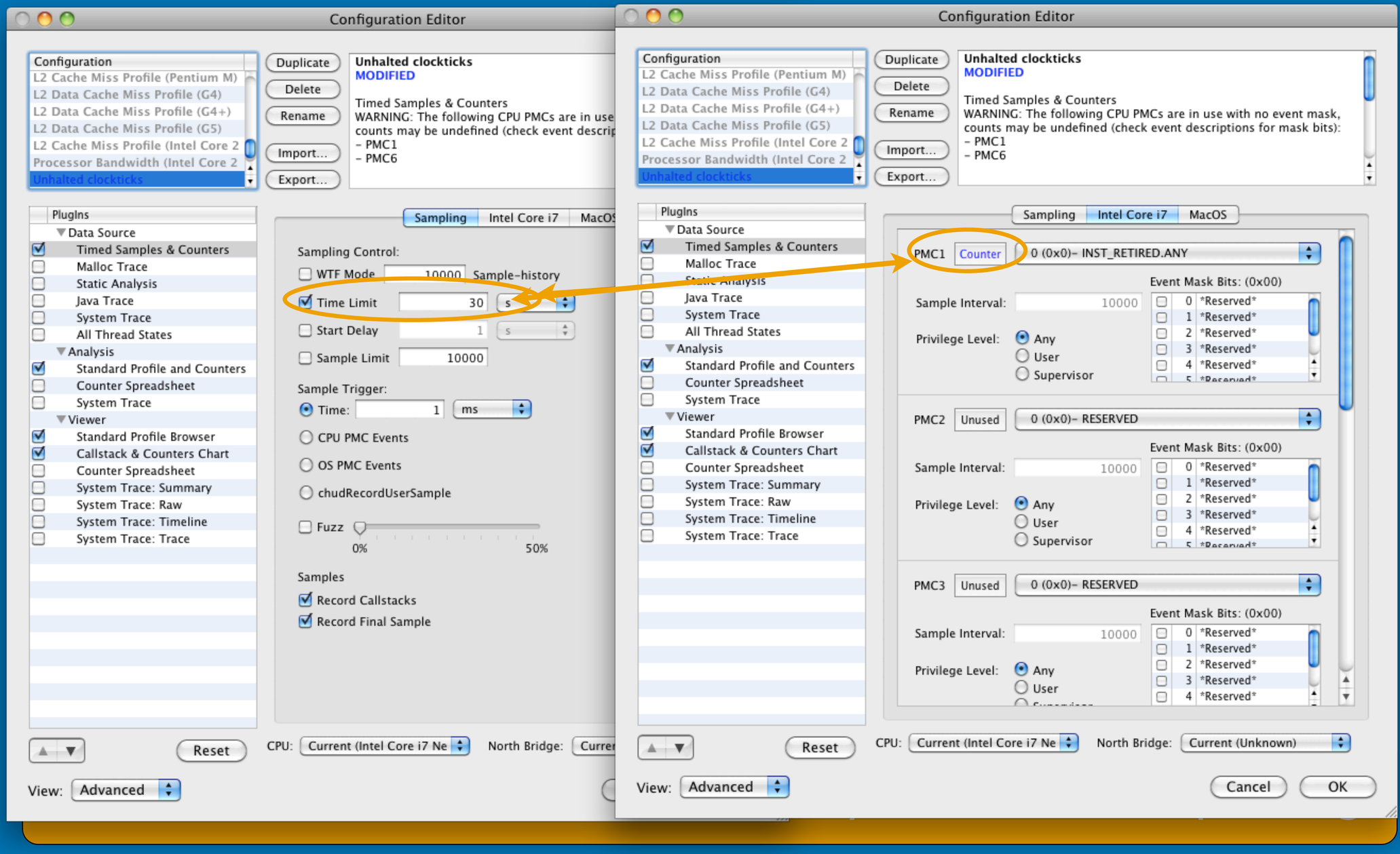
Demo Using Shark Advanced Configuration

Time-Based Sampling with Counters



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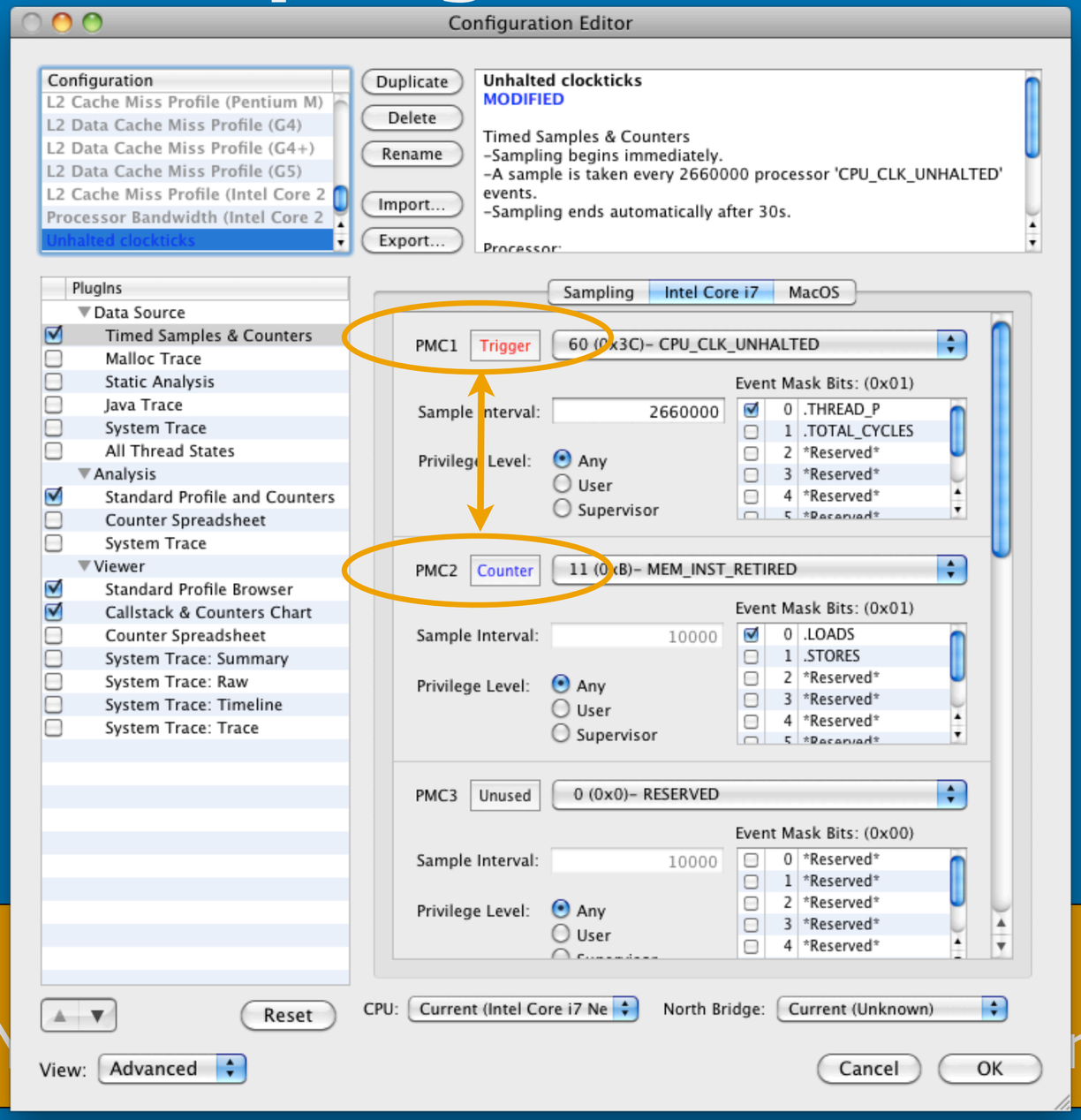

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Example of Statistical Sampling

- Two functions
  - Completely compute (no loads instructions)
  - Mostly load bound (L1D misses)
- Correct statistical sampling
  - ~ 75% of time in compute function
  - ~ 25% of time in load bound function
  - ~ 100% L1D misses in load bound function
  - ~ 0% L1D misses in the compute function

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Two Functions…

L1DRepl.cpp

L1DRepl.cpp:1 <No selected symbol>

```
30
31  unsigned int mem[40*1024]; // 4 * 100 * 1024 = 80KB
32
33  int L1_CacheMiss_function_25percent() __attribute__ ((noinline));
34  int L1_CacheMiss_function_25percent()
35  {
36      int* ptr = (int*) &(mem[0]);
37      unsigned int count = 16;
38      __asm__ __volatile__ ("mov $300, %%edi;"
39                            "loop3:;"
40                            "mov %2, %%edx;"
41                            "mov $16, %0;"
42                            "loop2:;"
43                            "mov (%%edx), %%ecx;"
44                            "addl $4096,%%edx;"
45                            "dec %0 ;"
46                            "jnz loop2;"
47                            "dec %%edi;"
48                            "jnz loop3;": "=r"(count) : "0"(count), "r"(ptr) : "%ecx", "%edx", "%edi" );
49
50      return count;
51  }
52
53
```

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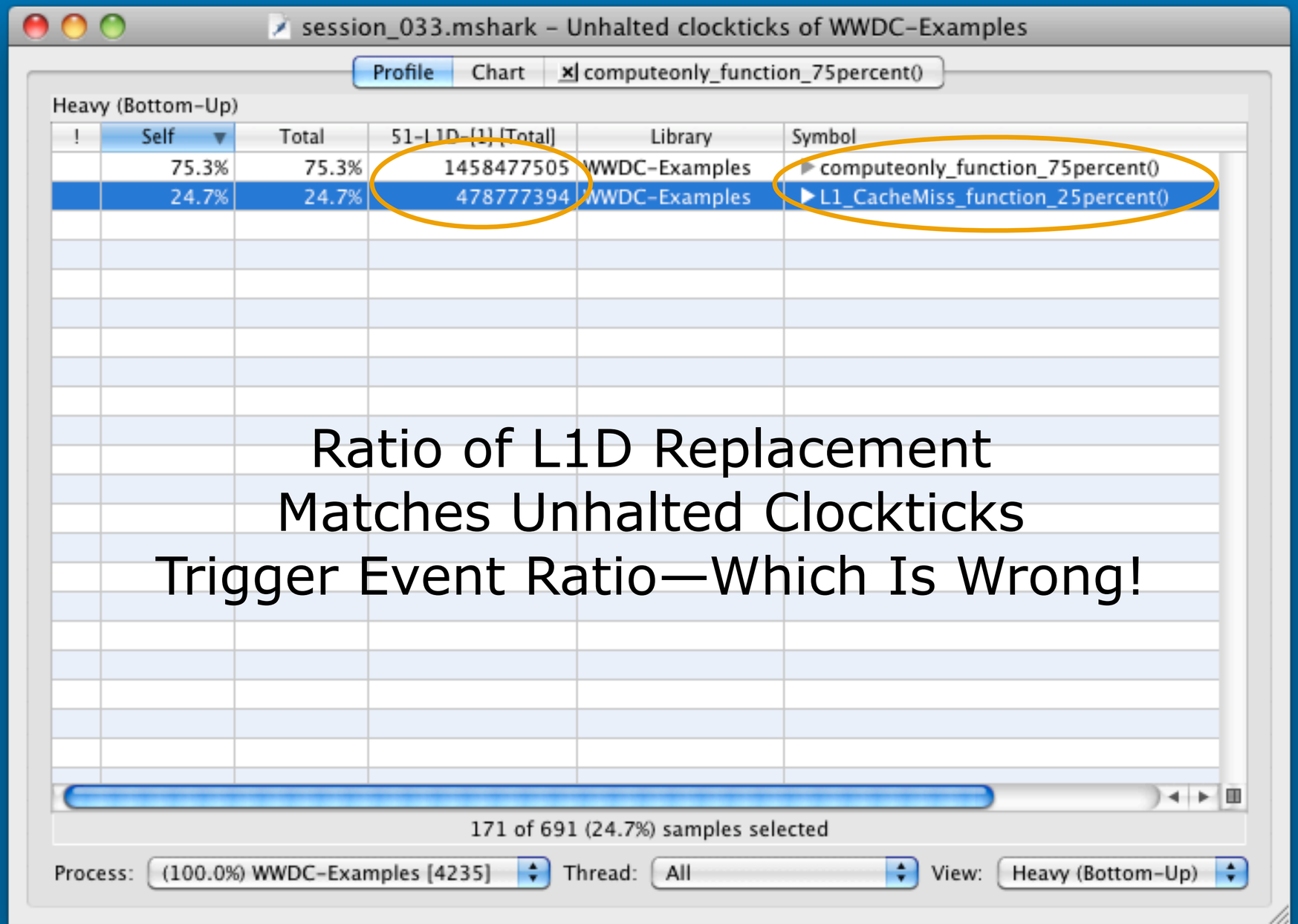
Trigger Data with Counter Data



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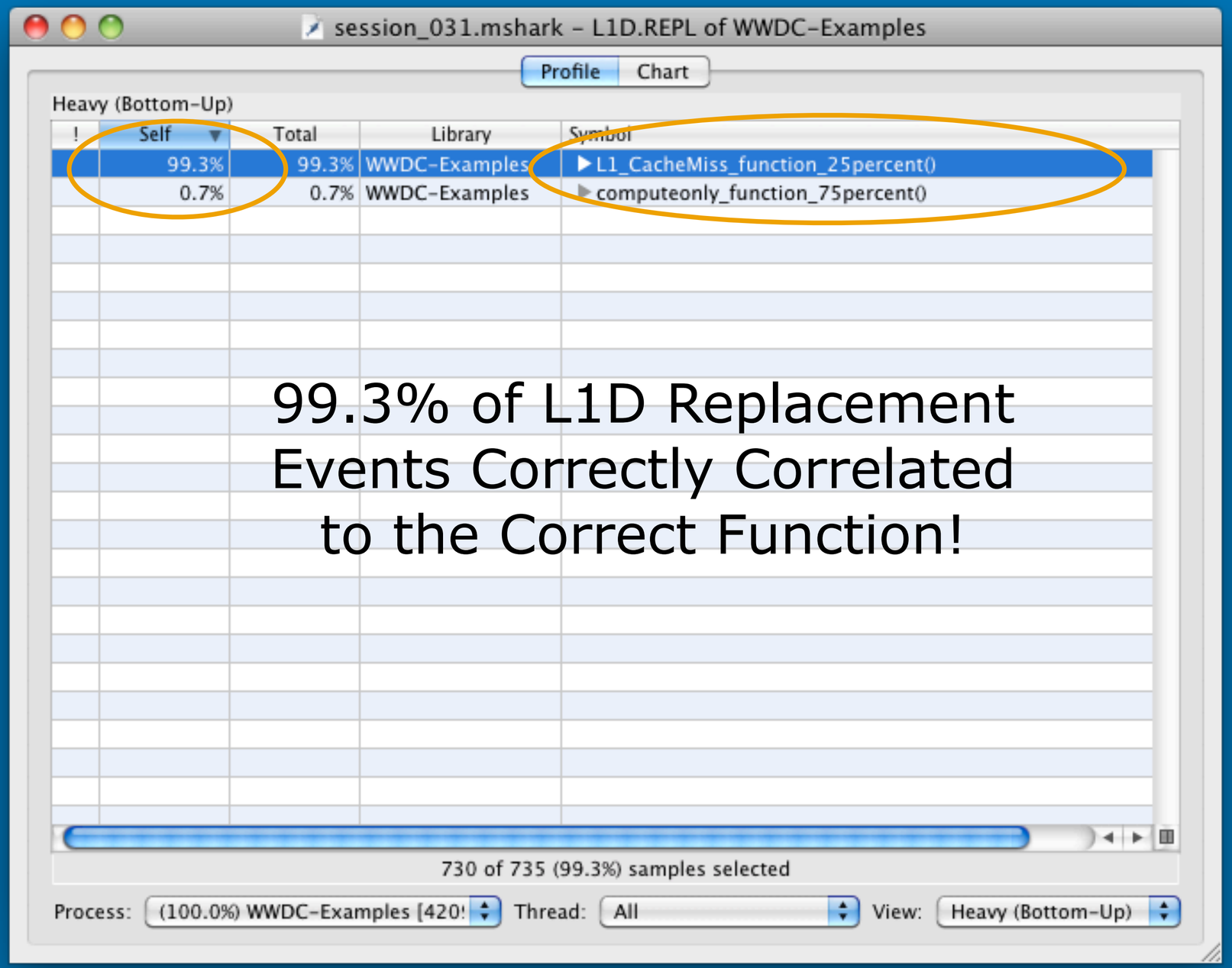
Trigger Only on L1D Replacement



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Trigger Only on L1D Replacement

session_031.mshark – L1D.REPL of WWDC-Examples

Profile | Chart | L1_CacheMiss_function_25percent()

0x1d86 0x1dc4 Source Assembly Both

Self	Address	Code	!	Comment	Source
	0x1d86	pushl %ebp	!	Inline	main.cpp:34
	0x1d87	movl $16, %eax			main.cpp:48
	0x1d8c	movl %esp, %ebp			main.cpp:34
	0x1d8e	subl $8, %esp			main.cpp:34
	0x1d91	movl %ebx, (%esp)			main.cpp:34
	0x1d94	movl $8288, %ebx			main.cpp:36
	0x1d99	movl %edi, +4(%esp)			main.cpp:34
	0x1d9d	movl $300, %edi			main.cpp:48
2.1%	0x1da2	movl %ebx, %edx		Loop start[1]	main.cpp:48
	0x1da4	movl $16, %eax			main.cpp:48
38.2%	0x1da9	movl (%edx), %ecx		Loop start[2]	main.cpp:48
54.2%	0x1dab	addl $4096, %edx			main.cpp:48
1.2%	0x1db1	decl %eax			main.cpp:48
	0x1db2	jnz 0x00001da9 <L1_C…		Loop end[2]	main.cpp:48
3.0%	0x1db8	decl %edi			main.cpp:48
0.8%	0x1db9	jnz 0x00001da2 <L1_Cache…		Loop end[1]	main.cpp:48
0.1%	0x1dbf	movl (%esp), %ebx			main.cpp:51
0.1%	0x1dc2	movl +4(%esp), %edi			main.cpp:51
	0x1dc6	leave			main.cpp:51
0.1%	0x1dc7	ret			main.cpp:51

396 of 730 (54.2%) self samples, 1 of 20 (5.0%) instructions selected

Asm Help

The only load instruction

Some Skid is Not Unusual

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What information can I get from processor events?

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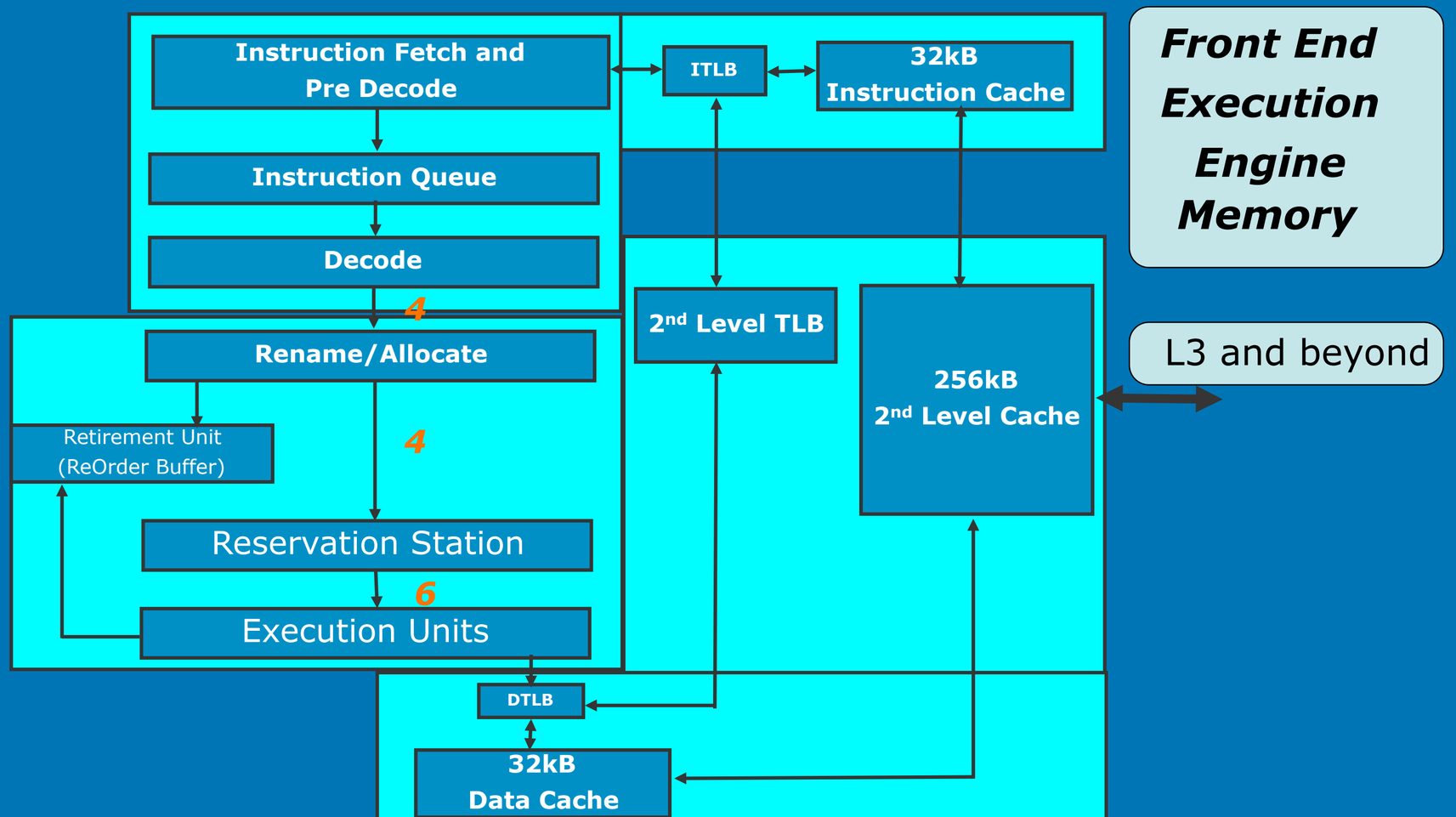
Intel® Microarchitecture Overview (Code Named Nehalem)



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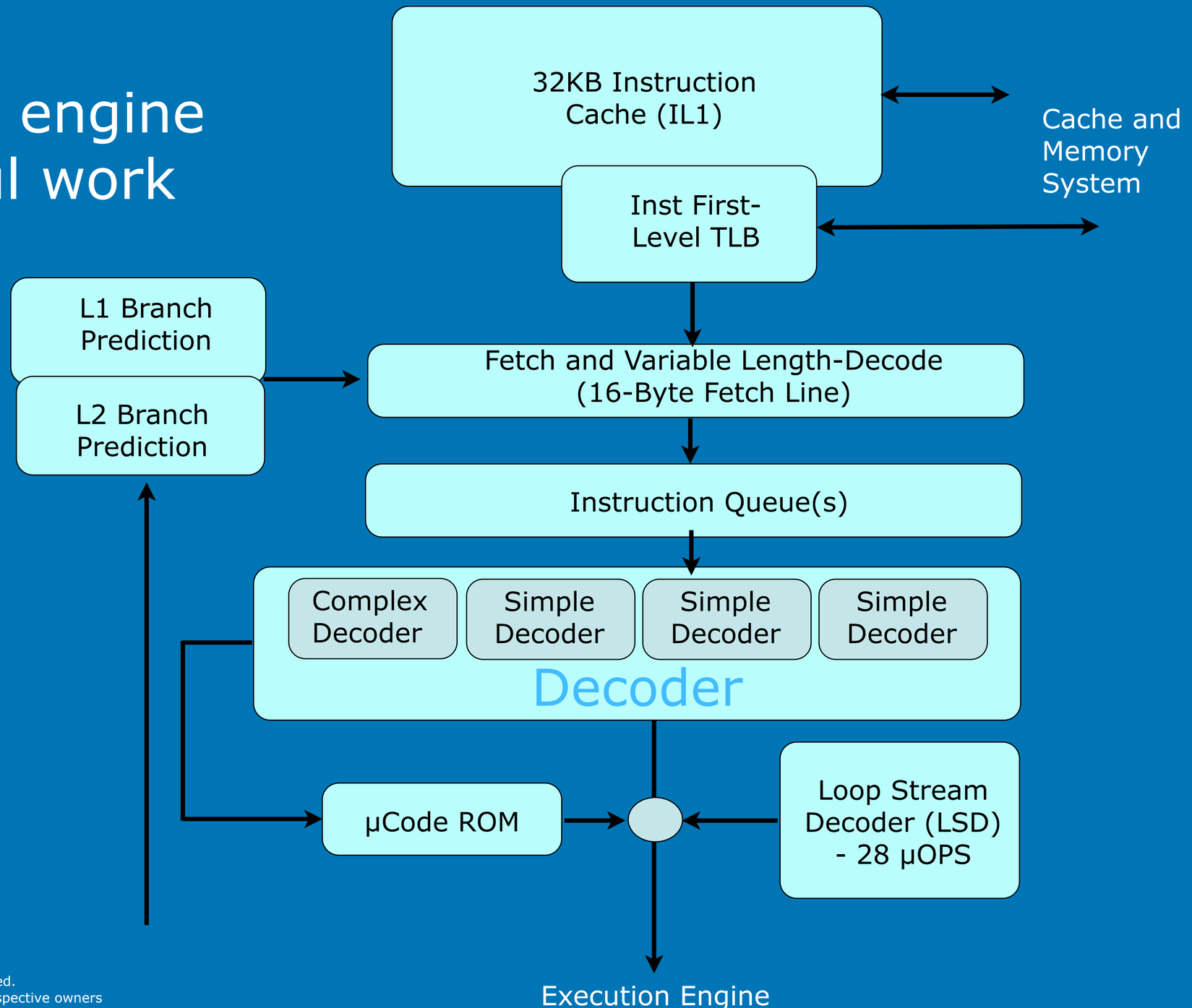
Front-End

Keep execution engine fed doing useful work



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Front-End

Keep execution engine fed doing useful work

L1I stall cycles

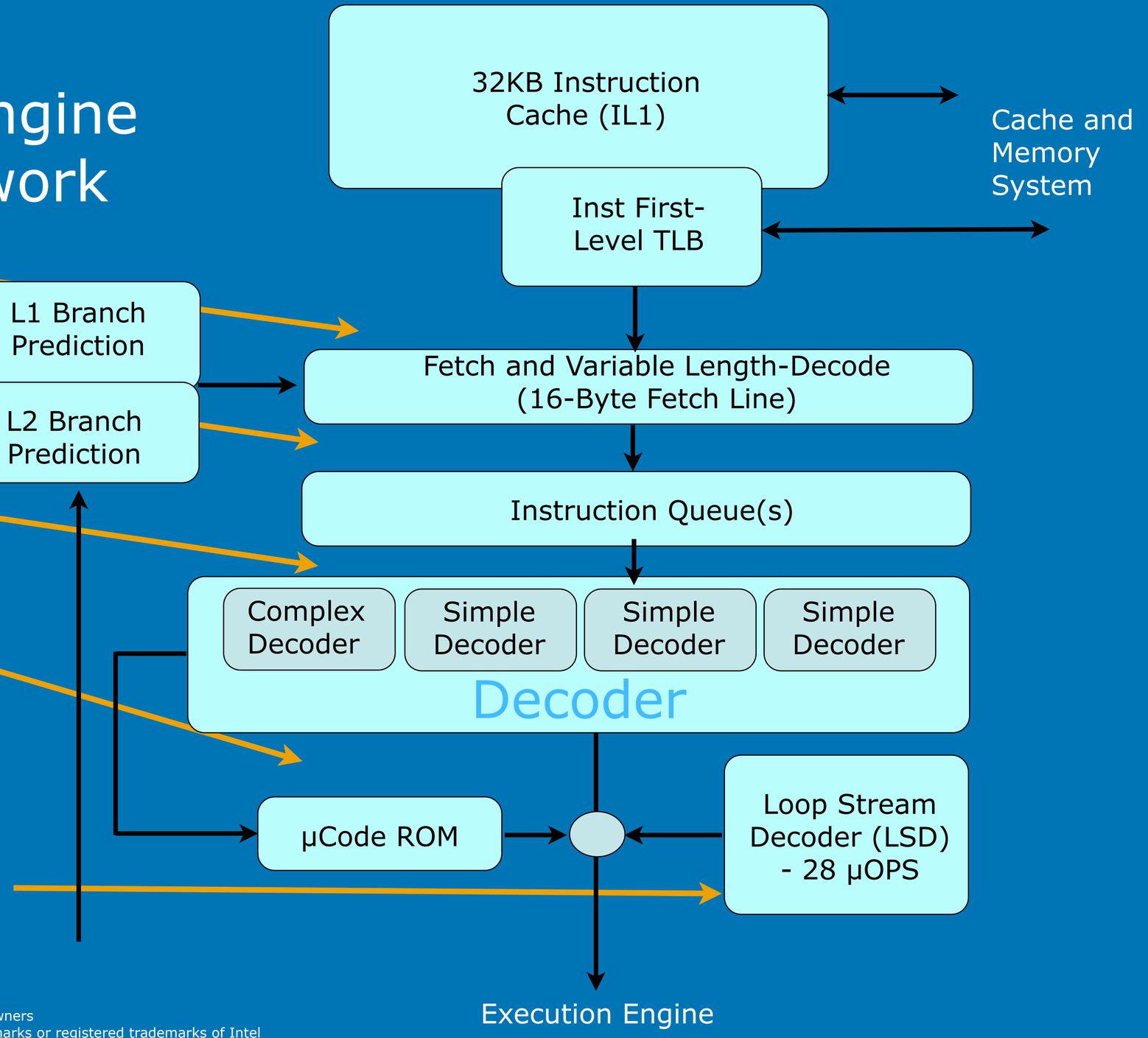
Instruction queue is full?

Instructions decoded

Complex instructions decoded

µOPS delivered from loop stream decoder

Many more…



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Front-End

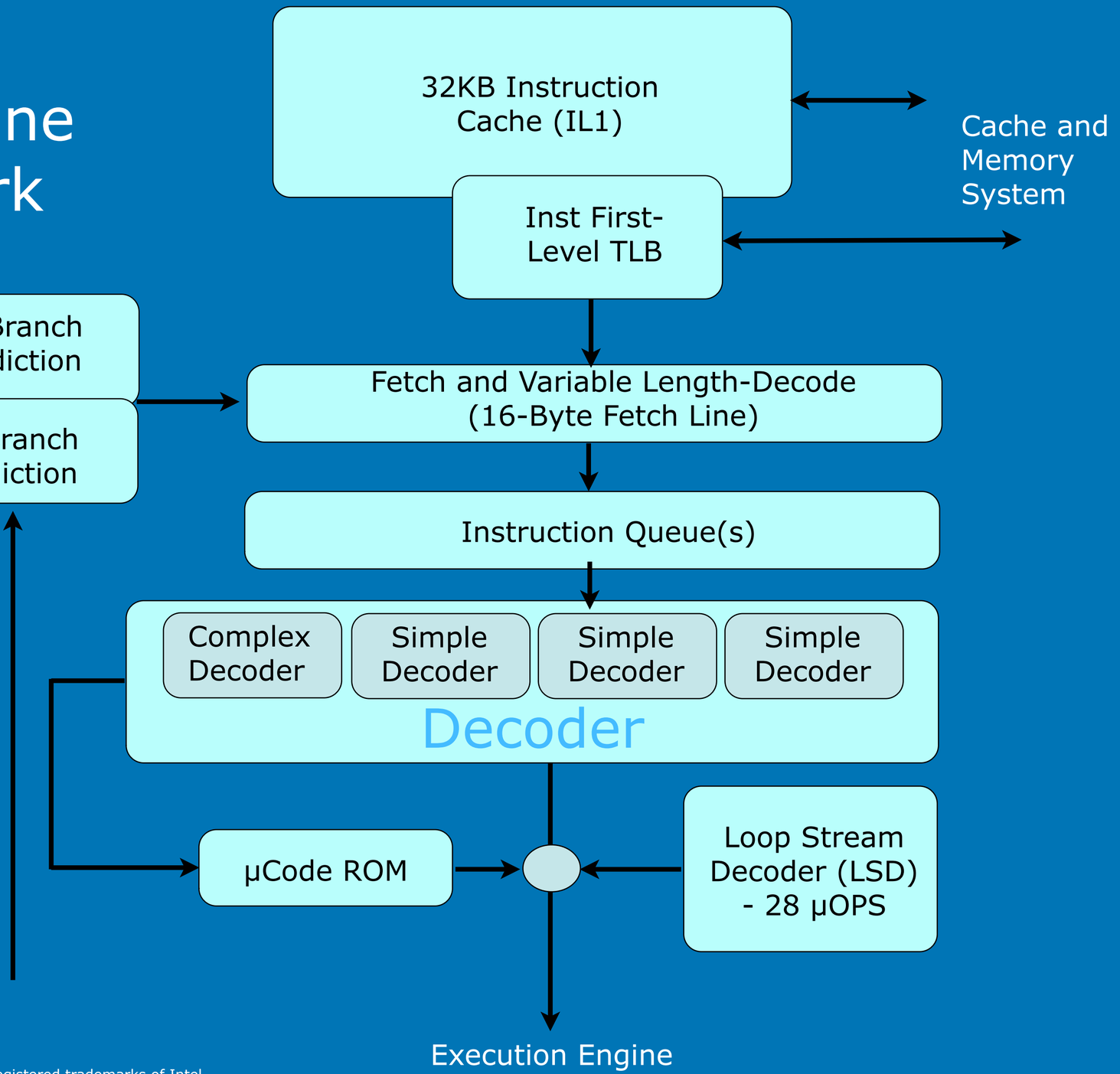
Keep execution engine fed doing useful work

Branch address clears

Branch instructions retired
-> Miss predicted or redicted
-> Taken or
-> Not taken

Branch prediction unit
-> Queue full

Many more…



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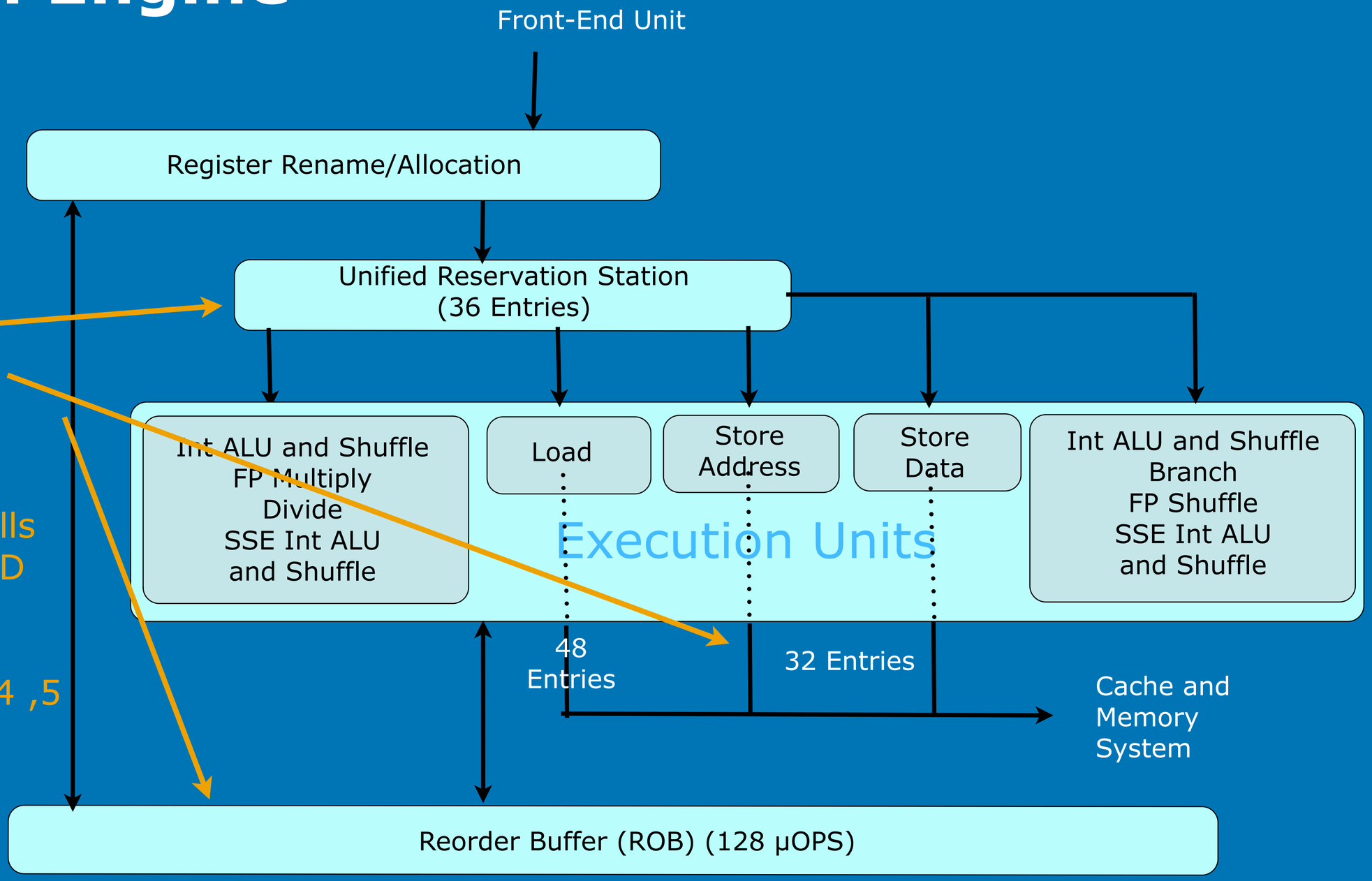
Execution Engine

Resource stalls
-> ROB full
-> RS full
-> LD/ST buffers stalls
-> ROB read port

Domain bypass stalls
-> FP, LD, and SIMD

RS dispatch ports
-> Port 0, 1, 2, 3, 4 ,5

Many more…



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Cache and Memory System

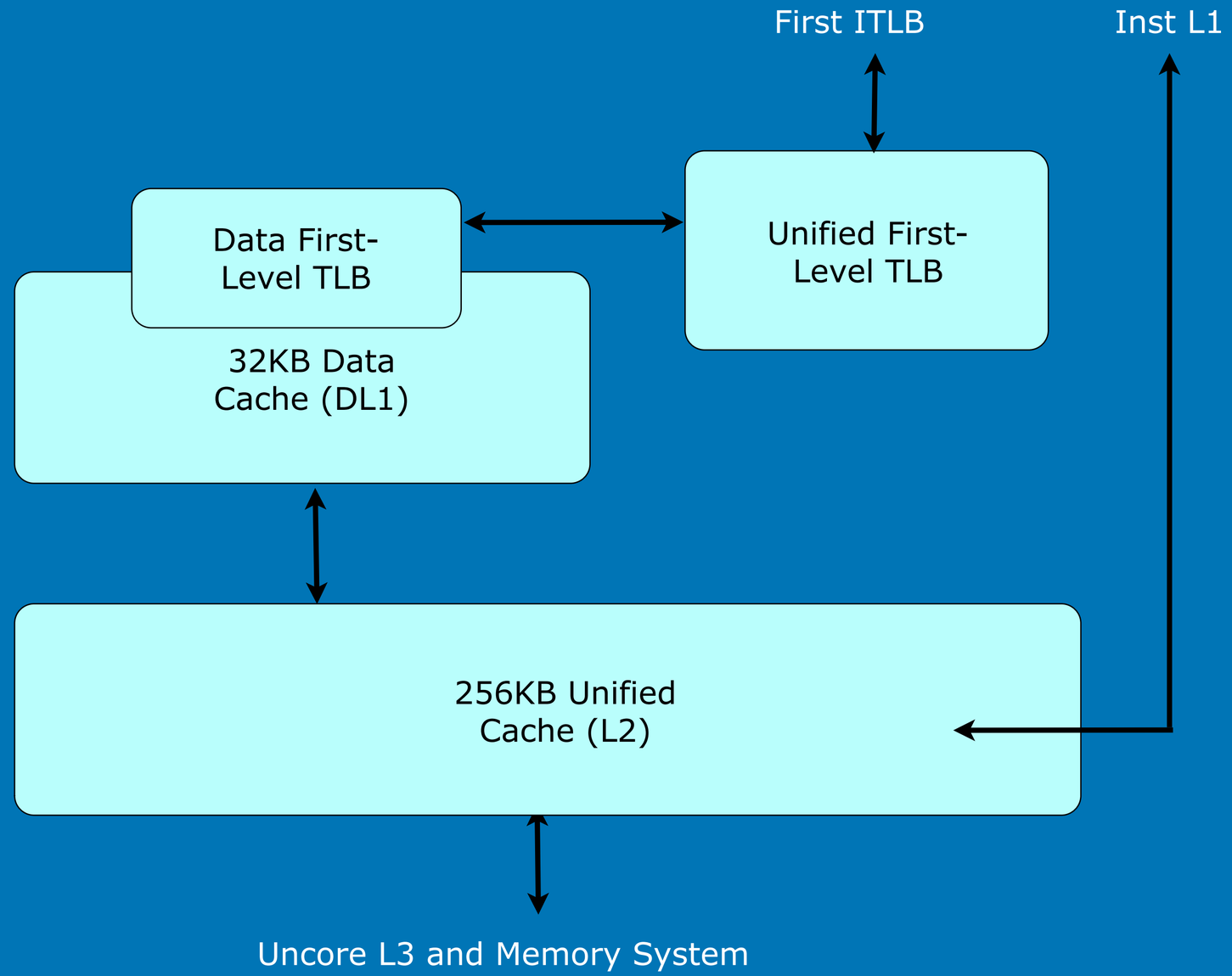
Num of L2 lines in
-> Due to demand
-> Due to prefetch

Num of L2 lines out
-> Due to demand
-> Due to prefetch

Memory inst retired
-> Loads
-> Stores

Memory uncore retired
-> Local DRAM
-> Remote DRAM

Many more…



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Lots of events to investigate
the IA architecture

Write small kernels and use events to
investigate the architecture

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Various Clock Cycle Domains

- Impact of turbo mode/thermal throttling on performance event cycle counts
  - Can affect expectations
- Be aware of the time domain
  - Especially when comparing event results
  - Using results in ratios

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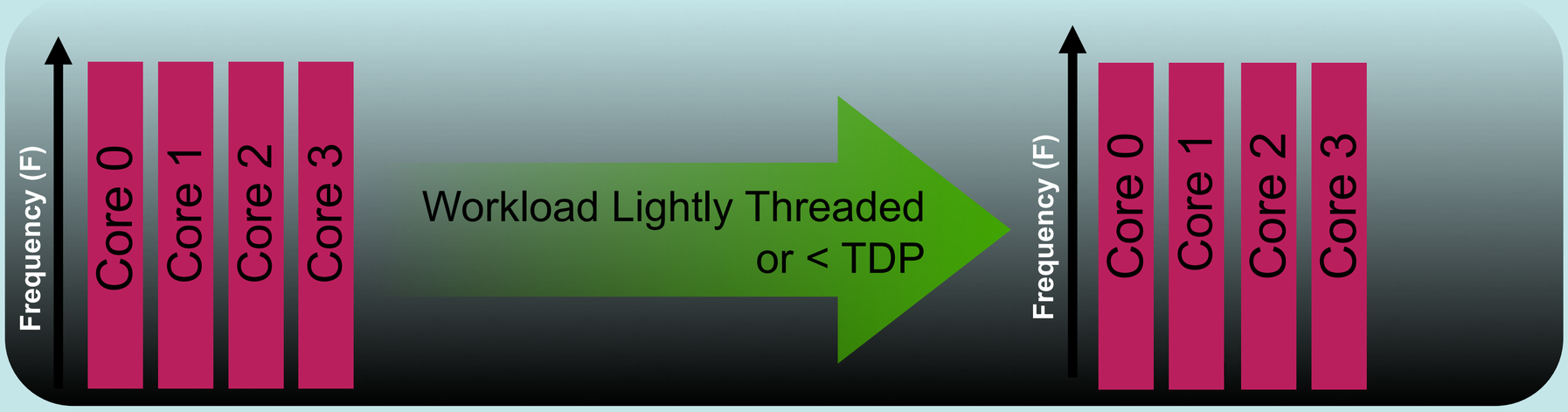
Various Clock Cycle Domains

Power Gating

Zero power for inactive cores

No Turbo



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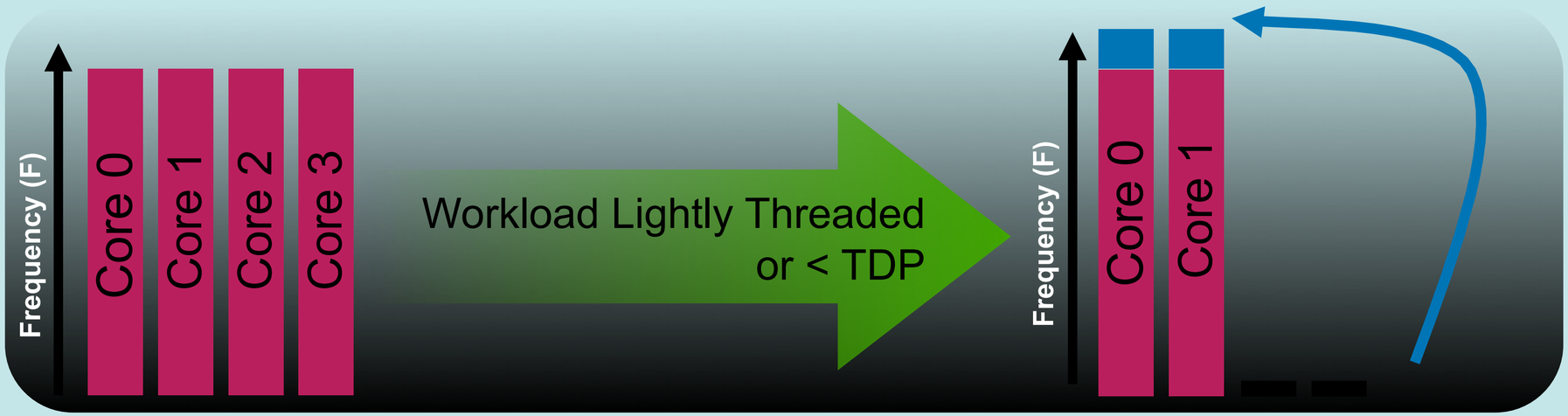
Various Clock Cycle Domains

<u>Power Gating</u>

Zero power for inactive cores

<u>Turbo Mode</u>

In response to workload adds additional performance bins within headroom



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Various Clock Cycle Domains

Counter	0	CPU_CLK_UNHALTED.REF_P	(Reference
CC=	ALL	PC=	0x1
cpu	0	398,240	(epc=0.000)
cpu	1	88,902	(epc=0.000)
cpu	2	55,773	(epc=0.000)
cpu	3	47,628	(epc=0.000)
cpu	4	382,038	(epc=0.000)
cpu	5	56,835	(epc=0.000)
cpu	6	373,907	(epc=0.000)
cpu	7	42,525	(epc=0.000)
cpu	8	43,717,122	(epc=0.050)
cpu	9	11,036	(epc=0.000)
cpu	10	3,108,140	(epc=0.004)
cpu	11	34,254	(epc=0.000)
cpu	12	176,508	(epc=0.000)
cpu	13	29,512	(epc=0.000)
cpu	14	381,519	(epc=0.000)
cpu	15	20,498	(epc=0.000)
Total	clock	cycles:	875,843,086

Counter	1	CPU_CLK_UNHALTED.THREAD_P	(Cycles
CC=	ALL	PC=	0x1
cpu	0	5,146,067	(epc=0.006)
cpu	1	1,304,842	(epc=0.001)
cpu	2	897,839	(epc=0.001)
cpu	3	797,365	(epc=0.001)
cpu	4	7,592,659	(epc=0.009)
cpu	5	864,512	(epc=0.001)
cpu	6	7,353,836	(epc=0.008)
cpu	7	636,886	(epc=0.001)
cpu	8	1,004,364,307	(epc=1.147)
cpu	9	177,918	(epc=0.000)
cpu	10	71,141,713	(epc=0.081)
cpu	11	685,958	(epc=0.001)
cpu	12	3,880,505	(epc=0.004)
cpu	13	572,013	(epc=0.001)
cpu	14	8,412,032	(epc=0.010)
cpu	15	371,926	(epc=0.000)
Total	clock	cycles:	875,843,027

Unhalted and Halted Clock Cycles (RDTSC)

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cpu		15		20,498	(epc=0.000)
Total	clock	cycles:			875,843,086

- Reference cycles x freq multiplier equals unhalted reference cycles
  - Taken on 2.66GHz Mac Pro (20x freq multiplier)
  - 43,717,122 * 20 = 874,342,440
  - In this case, no unhalted cycles for CPU 8

Unhalted Reference Clock Cycles

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cpu	14	8,412,032	(epc=0.010)
cpu	15	371,926	(epc=0.000)
Total	clock	cycles:	875,843,027

- All unhalted cycles independent of freq
  - In this case, CPU 8 has ~ 14.7% frequency upside

Unhalted Thread Clock Cycles

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cpu	15	371,926	(epc=0.000)
Total	clock	cycles:	875,843,027

- Other CPUs are mostly halted
  - In this case, CPU 3 is ~ .1% active

Unhalted Thread Clock Cycles

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Be sure to know what the event counts

Before you try to interpret the data!

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How to Interpret the Results?

- It “depends”
- Use ratios of events
- Understanding the performance bottleneck

You will get very BIG counts…
need to correlate with expectations—
Application and hardware!

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How to Get Started

- Start with basic performance characterization
  - Cycles per instruction (CPI)
  - Branch miss prediction per µOPS retired
  - L1 data cache miss rate
  - L2 cache demand miss rate
- Correlate with known constraints
  - Max CPI
  - L1/L2/LLC cache latency
  - Understanding of expected branch behavior
  - Compensate for turbo/thermal impacts

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How to Get Started

- Start with the bigger bottlenecks first
  - Memory/cache bandwidth
  - Execution units
  - Front-end/eecoder
- Beware of the cause and effect
  - Focus on the clog and not the symptom
- Start with simple events
  - Know what you are measuring
  - Events can be complex (be careful combining subevents)

Drill down using focus performance events—
Understand your workloads behavior!

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Summary

- Event monitoring is a powerful tool
  - Investigate/understand the architecture
  - Use to optimize your applications
  - Support simple to complex analyses
- More skillful the user…more useful the tool
  - Know the application
  - Know the architecture
  - Know the tools

Become your organizations expert using processor performance events!

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- Shark User Guide
- Intel® VTune™ Performance Analyzer

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